WHAT IS CLAIMED IS:

1. Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, the integrated circuit comprising means of distributing a mains voltage and means of generating an internal reference voltage lower than the mains voltage, characterized in that it comprises

means of connection to the mains voltage on the output, and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, taking into account the reference voltage.

2. Integrated circuit according to claim 1, characterized in that the predetermined voltage is equal to the reference voltage.

3. Integrated circuit according to claim 2, characterized in that, when the predetermined voltage is reached, the currents circulating in the means of connecting the mains voltage and the means of limiting and/or detecting the voltage are balanced.

4. Integrated circuit according to claim 2, characterized in that the connection means comprise a first power transistor.

5. Integrated circuit according to claim 4, characterized in that the drain of the primary transistor is connected to the output and its source to the mains voltage.

6. Integrated circuit according to claim 2, characterized in that the means of limiting the voltage comprise at least a second transistor controlled on its gate by the reference voltage.

7. Integrated circuit according to claim 6, characterized in that the gate of the second transistor is connected to the gate of a third transistor mounted in a diode at the reference voltage.

8. Integrated circuit according to claim 4, characterized in that the means of limiting the voltage comprise means of blocking the first transistor when the predetermined voltage is reached.

9. Integrated circuit according to claim 8, characterized in that the blocking means have first and second current mirrors connected to each other.

10. Integrated circuit according to claim 9, characterized in that the first current mirror delivers a blocking current when the predetermined voltage is reached on the output, and in that the

second mirror sends a copy of the blocking current to the gate of the first transistor, so as to block it.

11. Integrated circuit according to claim 4, characterized in that the gate of the first transistor is connected to a command input via a fourth transistor.

12. Integrated circuit according to claim 10, characterized in that the power of the third transistor is less than that of the transistors of the second mirror, so that the latter imposes its level on the third transistor when it delivers the copy of the blocking current.

13. Integrated circuit according to claim 1, characterized in that the output voltage corresponds to the logic level "1" of a USB connection.

14. Integrated circuit according to claim 1, characterized in that the reference voltage is used to supply the logic CMOS section of the integrated circuit.

15. Integrated circuit according to claim 1, characterized in that the reference voltage and/or the predetermined voltage have the value of 3 V, the mains voltage having a value of 5 V.

16. Communication module for the integrated circuit comprising means of delivering, on at least one output, a predetermined output voltage representative of a logic level, the integrated circuit comprise means of distributing a mains voltage and means of generating an internal reference voltage lower than the mains voltage, characterized in that it comprises

means of connecting the mains voltage to the output, and

means of limiting voltage at the output at the predetermined output voltage value, taking into account the reference voltage.

17. Integrated circuit according to claim 1, characterized in that, when the predetermined voltage is reached, the currents circulating in the means of connecting the mains voltage and the means of limiting and/or detecting the voltage are balanced.

18. Integrated circuit according to claim 1, characterized in that the connection means comprise a first power transistor.

19. Integrated circuit according to claim 18, characterized in that the drain of the primary transistor is connected to the output and its source to the mains voltage.

20. Integrated circuit according to claim 1, characterized in that the means of limiting the voltage comprise at least a second transistor controlled on its gate by the reference voltage.